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Docket No.: MICRON.214DDV1

October 17, 2005

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TRANSMITTAL LETTER

APPEAL BRIEF

Applicant	:	Liu, et al.
App. No	:	10/646,103
Filed	:	August 22, 2003
For	:	PASSIVATED MAGNETO-RESISTIVE BIT STRUCTURE AND PASSIVATION METHOD THEREFOR
Examiner	:	Marcos D. Pizarro Crespo
Art Unit	:	2814

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Michael S. Okamoto, Reg. No. 47,831

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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Dated: October 17, 2005

Michael S. Okamoto
Registration No. 47,831
Attorney of Record
Customer No. 20,995
(310) 551-3450

PAT-ABRIEFTRANS

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Sir:

In accordance with the Notice of Appeal filed June 17, 2005, Applicants (Appellants) submit this Appeal Brief.

TABLE OF CONTENTS

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I. REAL PARTY IN INTEREST

The real party of interest in the present application is Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

Pursuant to 37 C.F.R. § 41.37(c)(2), Appellants hereby notify the Board of Patent Appeals that Appellants, the Appellants Legal Representative, and the Assignee do not know of any appeals or interferences that will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are currently pending in the application, and are attached hereto as an appendix. All of the pending claims were finally rejected by the Examiner and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

Appellants amended Claim 8 in response to the first Office Action. No claims have been amended subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to magneto-resistive memories, and more particularly, to the passivation of magneto-resistive bit structures.

One aspect of the present invention is a method of passivating a magento-resistive bit 32a by encapsulating the top and side wall surface of the magneto-resistive bit 32a with a conductive etch stop barrier layer 36a. Reference numbers are to the present application unless indicated otherwise. Paragraphs [0023] to [0028] and Figures 5-10 illustrate an example of the method.

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Another aspect of the present invention includes a process for passivating a magneto-resistive bit structure characterized by the steps of: providing a GMR stack 32 upon a substrate 30; selectively patterning said GMR stack 32 to form at least one GMR bit 32a having a top surface and side walls; providing a conductive etch stop barrier layer 36 that encapsulates the patterned GMR stack 32a including the top surface and side walls of the GMR bit 32a; and selectively patterning said barrier layer 36 so that the edges of the barrier layer 36a extend out past the edges of the GMR bit 32a. Paragraphs [0022] to [0028] and Figures 4-10 illustrate an example of the method.

Another aspect of the present invention includes a process for passivating a patterned magneto-resistive bit structure in a magneto-resistive memory, the process comprising: providing a substrate 30 with the patterned magneto-resistive bit structure 32a, the patterned magneto-resistive bit structure 32a having a top surface and side walls; forming a conductive etch stop barrier layer 36 over the substrate 30 with the patterned magneto-resistive bit structure 32a, the conductive etch stop barrier layer 36 covering the top surface of the magneto-resistive bit structure and the side walls of the magneto-resistive bit structure 36; and patterning the conductive etch stop barrier layer 36 such that the conductive etch stop barrier layer 36 is removed from portions of the substrate 30, but where the conductive etch stop barrier layer 36a remains on the top surface and around the side walls of the magneto-resistive bit structure 32a. Paragraphs [0023] to [0028] and Figures 5-10 illustrate an example of the method.

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VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A) Independent Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,861,328 to Tehrani, et al ("Tehrani").

B) Independent Claim 8 was rejected under 35 U.S.C. § 102(b) as being anticipated by Tehrani.

C) Independent Claim 12 was rejected under 35 U.S.C. § 102(b) as being anticipated by Tehrani.

D) Dependent Claims 3, 6, 15, and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tehrani in view of U.S. Patent No. 5,496,759 to Yue, et al ("Yue").

E) Dependent Claims 2-7, 9-11 and 13-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tehrani or under 35 U.S.C. § 103(a) as being unpatentable over Tehrani in view of Yue.

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VII. ARGUMENT

Discussion of the Tehrani Reference Relied Upon by the Examiner

Appellants and the Examiner disagree on the teachings of Tehrani. Appellants believe that Tehrani teaches two distinct processes, i.e., a process with a dielectric barrier and a process suitable for a conductive etch stop barrier layer, but only illustrates the process with the dielectric barrier in the figures. Appellants believe that the Examiner is improperly mixing the teachings of the process suitable for the conductive barrier (not illustrated) with the teachings of the process with the dielectric barrier (illustrated).

The claimed invention requires sidewalls of a magnetoresistive bit to be encapsulated by a conductive etch stop barrier layer. The Examiner applies a conductive barrier teaching of Tehrani and improperly combines it with another Tehrani process in which sidewalls of a magnetic bit are exposed prior to forming a dielectric barrier. In fact, the two Tehrani processes are separate and incompatible.

The process with the dielectric barrier is illustrated in Figures 5, 6, and 7 is described from Col. 4, line 66 to Col. 5, line 53. For example, in the dielectric barrier process, "via openings 47 are formed... as illustrated in FIG. 6" (Col. 5, lines 22-24) and "via openings 50 are formed," (Figure 7 and Col. 5, lines 34-35) in separate operations.

The process with the conductive barrier is described from Col. 5, line 54 to Col. 6, line 12 starting with "[i]n a somewhat different process," and is not shown. In contrast to the dielectric barrier process, with respect to the process with the conductive barrier Tehrani states "vias 47 and 50 are formed in a single operation." Tehrani explicitly acknowledges that two distinct processes are taught by the use of the term "either" in: "[a]fter the formation of vias 47 and 50, by either of the above described means," (Col. 6, lines 13-14) (emphasis added), which indicates two exclusive alternatives.

Tehrani admonishes against a combination of the two processes. With respect to the illustrated dielectric barrier process, "[v]ia openings 50 may overlap GMR memory element 41,

that is, vias 50 may extend outside or intersect the end of GMR element 41," (Col. 5, lines 36-38) In contrast, with respect to the non-illustrated conductive barrier process, Tehrani states that "[v]ia opening 50 must be enclosed by GMR memory element 41, that is the contact may not extend outside the ends of GMR memory element 41 to protect element 41 from the resist stripping processes and other oxidizing or corrosive agents," (Col. 5, lines 58-62).

Certain other aspects of the processes are also not compatible with each other and cannot be interchanged. For example, the dielectric barrier of Tehrani's dielectric barrier process must be selectively removed for contact, whereas a conductive layer remains in place for the contact. With respect to the dielectric barrier, Tehrani teaches that "[t]he barrier layer is removed with fluorine based chemistries, or other chemistries, which do not damage (oxidize or corrode) GMR element 41," (Col. 5, lines 48-50). By contrast, "[i]n instances where the etch stop and passivation layer is electrically conductive, contact metal (to be explained presently) can simply be deposited in contact therewith in vias 50," (Col. 6, lines 9-12) (emphasis added).

Appellants further submit that it is only in the context of the second process that is not illustrated in the figures that Tehrani describes conductive materials such as CrSi for the etch stop and passivation layer, see Col. 5, line 67 to Col. 6, line 1.

A) Claim 1 is not anticipated by Tehrani, et al.

The Examiner asserts that "Tehrani shows (see, *e.g.*, figs. 4-8) all aspects of the instant invention including a process for passivating a magneto-resistive bit 41 having a top surface and side walls characterized by encapsulating the top and side wall surfaces of the bit 41 with a conductive etch stop layer."

The Examiner appears to cite Figures 4-8 of Tehrani as teaching "encapsulating the top and side wall surfaces of a magneto-resistive bit with a conductive etch stop barrier layer." As previously discussed, Tehrani teaches two distinct processes, one with a dielectric barrier and one with a conductive barrier. In Tehrani's dielectric barrier process, Tehrani teaches using silicon

nitride as a barrier, a second layer of SiO_2, and an optional third layer of AlO or AlN as an etch stop layer for the dielectric cap 45 (Col. 5, lines 3-21). None of these materials are conductive.

By contrast, Tehrani teaches the use of CrSi as an "etch stop and passivation layer," (Col. 5, line 67 to Col. 6, line 1), in connection with a process suitable for a conductive barrier that Tehrani refers to as "a somewhat different process," (Col. 5, line 54). CrSi is conductive. With this conductive barrier process, Tehrani states "[v]ia opening 50 must be enclosed by GMR memory element 41, that is the contact may not extend outside the ends of GMR memory element 41," see Col. 5, lines 58-60 (emphasis added). As described by Tehrani, "where the etch stop and passivation layer is electrically conductive, contact metal (to be explained presently) can simply be deposited in contact therewith in vias 50," (Col. 6, lines 9-12). Thus, when Tehrani describes a "conductive etch stop barrier layer," the layer explicitly does not encapsulate the side walls.

Thus, the Examiner's characterization of Tehrani is either factually incorrect, or it represents a legally-unsupported modification (or combination of embodiments) of Tehrani. Appellants further note that if the Examiner is modifying Tehrani, the appropriate statutory basis for a rejection of Claim 1 could rest only on 35 U.S.C. § 103. However, Appellants further note that "[e]ven when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference." *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2D 1313. Appellants respectfully submit that there has been no showing of a suggestion or motivation to modify the teachings of Tehrani, nor could the Examiner show such motivation, given Tehrani's teaching away from exposing the sidewalls to a conductive barrier. Accordingly, Appellants submit that Claim 1 is patentably distinguished over the prior art and the Examiner's rejection of Claim 1 should be reversed by the Board.

B) Claim 8 is not anticipated by Tehrani

The Examiner asserts that "Tehrani shows (see, *e.g.*, figs. 4-8) all aspects of the instant invention including ... [p]roviding a conductive etch-stop barrier layer that encapsulates the patterned GMR stack 35 including the top surface and sidewalls of the bit (see, *e.g.*, fig. 5) [and] [s]electively patterning the etch-stop layer so that edges of the layer extend out past the edges of the GMR bit 41 (see, *e.g.*, fig. 6)."

As previously discussed, Tehrani teaches two distinct processes, one with a dielectric barrier and one with a conductive barrier. In Tehrani's dielectric barrier process, Tehrani teaches using non-conductive materials, such as silicon nitride as a barrier, a second layer of SiO_2, and an optional third layer of AlO or AlN as an etch stop layer for the dielectric cap 45 (Col. 5, lines 3-21).

Tehrani teaches the use of CrSi as an "etch stop and passivation layer," (Col. 5, line 67 to Col. 6, line 1), in connection with the conductive barrier process that Tehrani refers to as "a somewhat different process," (Col. 5, line 54). With this process, Tehrani states "[v]ia opening 50 must be enclosed by GMR memory element 41, that is the contact may not extend outside the ends of GMR memory element 41," see Col. 5, lines 58-60 (emphasis added). Tehrani further describes that "where the etch stop and passivation layer is electrically conductive, contact metal (to be explained presently) can simply be deposited in contact therewith in vias 50," (Col. 6, lines 9-12). Thus, Tehrani's "conductive etch stop barrier layer" does not encapsulate the side walls.

In addition, the Examiner relies on Tehrani's Figure 6 as support for the assertion that Tehrani teaches "selectively patterning the etch-stop layer so that edges of the layer extend out past the edges of the GMR bit 41 (see, *e.g.*, fig. 6)." Figure 6 applies only to Tehrani's dielectric barrier process and not to Tehrani's conductive barrier process. Appellants note that Figure 6 illustrates only the forming of "via openings 47," see Col. 5, line 22. Via openings 50 are not present until later. "Subsequent to the patterning and etching of vias 47, via openings 50 are formed through dielectric cap 45," see Col. 5, lines 34-36. By contrast, with respect to the

process, "[i]n a somewhat different process, vias 47 and 50 are formed in a single operation," see Col. 5, lines 54-55. Accordingly, in the conductive barrier process described by Tehrani in connection with materials such CrSi, Figure 6 does not apply.

Thus, the Examiner's characterization of Tehrani is either factually incorrect, or it represents a legally-unsupported modification (or combination of embodiments) of Tehrani. Appellants respectfully submit that there has been no showing of a suggestion or motivation to modify the teachings of Tehrani, nor could there be given Tehrani's teaching away from exposing the sidewalls to a conductive barrier. Accordingly, Appellants submit that Claim 8 is patentably distinguished over the prior art and the Examiner's rejection of Claim 8 should be reversed by the Board.

C) Claim 12 is not anticipated by Tehrani

The Examiner asserts that "Tehrani shows (see, *e.g.*, figs. 4-8) all aspects of the instant invention including "[f]orming a conductive etch-stop barrier layer over the substrate, the etch-stop layer covering the top surface and side walls of the bit structure (see, *e.g.*, fig. 5) [and] [p]atterning the etch-stop layer such that it is removed from portions of the substrate but it remains on the top surface and around the side walls of the bit structure (see, *e.g.*, fig. 6)."

As previously discussed, Tehrani teaches two distinct processes. In Tehrani's illustrated dielectric barrier process, Tehrani teaches using non-conductive materials, such as silicon nitride as a barrier, a second layer of SiO_2, and an optional third layer of AlO or AlN as an etch stop layer for the dielectric cap 45 (See Col. 5, lines 3-21).

Tehrani teaches the use of CrSi as an "etch stop and passivation layer," (Col. 5, line 67 to Col. 6, line 1), in connection with a non-illustrated conductive barrier process that Tehrani refers to as "a somewhat different process," (Col. 5, line 54). With this non-illustrated conductive barrier process, Tehrani states "[v]ia opening 50 must be enclosed by GMR memory element 41, that is the contact may not extend outside the ends of GMR memory element 41," (Col. 5, lines

58-60) (emphasis added). Into these via openings, Tehrani further describes that "where the etch stop and passivation layer is electrically conductive, contact metal (to be explained presently) can simply be deposited in contact therewith in vias 50," (Col. 6, lines 9-12). Thus, when Tehrani describes a "conductive etch stop barrier layer," it does not encapsulate the side walls.

In addition, the Examiner relies on Tehrani's Figure 6 as support for the assertion that Tehrani teaches "[p]atterning the etch-stop layer such that it is removed from portions of the substrate but it remains on the top surface and around the side walls of the bit structure (see, *e.g.*, fig. 6)." As discussed earlier in connection with the rejection of Claim 8, Figure 6 does not apply to the non-illustrated conductive barrier process described by Tehrani with materials such as CrSi as the "vias 47 and 50 are formed in a single operation," (Col. 5, lines 54-55) for the non-illustrated conductive barrier process.

Thus, the Examiner's characterization of Tehrani is either factually incorrect, or it represents a legally-unsupported modification (or combination of embodiments) of Tehrani. Appellants respectfully submit that there has been no showing of a suggestion or motivation to modify the teachings of Tehrani, nor could there be given Tehrani's teaching away from exposing the sidewalls to a conductive barrier. Accordingly, Appellants submit that Claim 12 is patentably distinguished over the prior art and the Examiner's rejection of Claim 12 should be reversed by the Board.

D) Claims 3, 6, 15, and 18 are not obvious over Tehrani in view of Yue

The Examiner acknowledges that Tehrani does not "specify the thickness of the etch-stop layer" in rejecting Claims 3 and 15. The Examiner uses Yue to provide the missing thickness element, and states that "[s]ince the applicants have not established the criticality ... of the etch-stop thickness... it would have been obvious to one of ordinary skill in the art to use these values in the device of Tehrani." The Examiner also acknowledges that Tehrani does not teach or suggest a thickness for a diffusion barrier of tantalum in rejecting Claims 6 and 18. The

Examiner also uses Yue to provide the missing thickness element for the tantalum layer, and asserts that "[t]he specification did not describe the critical nature of the claimed thickness or any unexpected results arising therefrom."

The thickness of a chrome-silicon (CrSi) layer and/or a tantalum (Ta) layer is important, as the thickness relates to the resistivity of material that is shunting (electrically in parallel with) the magneto-resistive bit.

As discussed for example with respect to Claim 1, Tehrani does not teach or suggest a conductive encapsulation of surfaces including the "side wall surfaces of a magneto-resistive bit with a conductive etch stop barrier layer" as claimed. Accordingly, the thickness is not important to Tehrani because where Tehrani uses a conductive barrier, it does not shunt Tehrani's bit.

Yue also does not teach a configuration using a conductive encapsulation present along the side walls, i.e., shunting or in parallel with the magneto-resistive bit. Accordingly, the thickness limitations of Yue are not applicable to the encapsulation along side walls.

The resistance of a conductive material (CrSi or Ta) is approximately a function of the bulk resistivity of the material multiplied by the length of the distance through which current travels through the material, divided by the cross-sectional area of the material through which current passes. The thickness of the CrSi layer or of the Ta layer further relates to the cross-sectional area. If the thickness of the CrSi layer or the Ta layer is too thick, the cross-sectional area becomes large, and the side walls of the magneto-resistive bit are effectively shorted by the CrSi layer. In paragraph [0024], Appellants described:

> As a barrier layer any etch stop material can be used which has a bulk resistivity low enough to allow sense line contact and high enough so that shunting will be negligible. CrSi is preferred. If desired, a thin Ta or TaN diffusion barrier can be deposited between the above-described barrier layer and the GMR stack to prevent intermixing. Figure 6 shows a barrier layer 36, made up of a 300 Å CrSi layer on a 100 Å Ta layer, deposited upon patterned GMR stack 32a and SiN substrate 30.

Thus, the Examiner's reliance on thicknesses for CrSi layers or for Ta layers that are used elsewhere from side walls is not applicable to CrSi or Ta present on side walls because in the prior art, the CrSi or Ta layers are not shunting or in parallel with a magneto-resistive bit. Thus, the criticality of thickness was not recognized in the prior art. Accordingly, the combination of Tehrani and Yue does not teach or suggest Claims 3, 6, 15, or 18. Accordingly, Appellants submit that these claims are patentably distinguished over the prior art and the Examiner's rejection of Claims 3, 6, 15, and 18 should be reversed by the Board.

E) Dependent Claims 2-7, 9-11 and 13-20

The Examiner rejects Claims 2, 4, 8-9, 13-14, 16-17, and 19-20 under 35 U.S.C. § 102(b) as being anticipated by Tehrani. The Examiner rejects Claims 3, 5-7, 10, 11, 15, and 18 as obvious over Tehrani in view of Yue.

As discussed for example with respect to Claim 1, Tehrani does not teach or suggest a conductive encapsulation of surfaces including the "side wall surfaces of a magneto-resistive bit with a conductive etch stop barrier layer." Yue further does not teach a configuration using a conductive material along the side walls, i.e., shunting or in parallel with the magneto-resistive bit, and thus fails to provide the missing element.

Therefore, the teachings of Tehrani alone or in combination with Yue, fail to "each and every element" as required by 35 U.S.C. § 102(b) or all the claim limitations as required for a *prima facia* case of obviousness under 35 U.S.C. § 103(a).

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VIII. CLAIMS APPENDIX

1. A process for passivating a magneto-resistive bit having a top surface and side walls characterized by encapsulating the top and side wall surfaces of a magneto-resistive bit with a conductive etch stop barrier layer.

2. The process as defined in Claim 1, wherein the conductive etch stop barrier layer comprises CrSi.

3. The process as defined in Claim 2, wherein the conductive etch stop barrier layer is about 300 Å.

4. The process as defined in Claim 1, further comprising forming a diffusion barrier between the conductive etch stop barrier layer and the top surface and side walls of the magneto-resistive bit.

5. The process as defined in Claim 3, wherein the diffusion barrier comprises Ta.

6. The process as defined in Claim 5, wherein the diffusion barrier is about 100 Å in thickness.

7. The process as defined in Claim 3, wherein the diffusion barrier comprises TaN.

8. A process for passivating a magneto-resistive bit structure characterized by the steps of:

providing a GMR stack upon a substrate;

selectively patterning said GMR stack to form at least one GMR bit having a top surface and side walls;

providing a conductive etch stop barrier layer that encapsulates the patterned GMR stack including the top surface and side walls of the GMR bit; and

selectively patterning said barrier layer so that the edges of the barrier layer extend out past the edges of the GMR bit.

9. The process as defined in Claim 8, further comprising forming a diffusion barrier between the etch stop barrier layer and the patterned GMR stack.

10. The process as defined in Claim 8, wherein selectively patterning the barrier layer further comprises:

forming a dielectric layer upon the barrier layer;

removing parts of the dielectric layer to expose portions of the barrier layer to be removed; and

ion milling to remove the exposed portions of the barrier layer to selectively pattern the barrier layer.

11. The process as defined in Claim 10, wherein removing comprises reactive ion etching.

12. A process for passivating a patterned magneto-resistive bit structure in a magneto-resistive memory, the process comprising:

providing a substrate with the patterned magneto-resistive bit structure, the patterned magneto-resistive bit structure having a top surface and side walls;

forming a conductive etch stop barrier layer over the substrate with the patterned magneto-resistive bit structure, the conductive etch stop barrier layer covering the top surface of the magneto-resistive bit structure and the side walls of the magneto-resistive bit structure; and

patterning the conductive etch stop barrier layer such that the conductive etch stop barrier layer is removed from portions of the substrate, but where the conductive etch stop barrier layer remains on the top surface and around the side walls of the magneto-resistive bit structure.

13. The process as defined in Claim 12, wherein the substrate further comprises a monolithic integrated circuit.

14. The process as defined in Claim 12, wherein the conductive etch stop barrier layer comprises CrSi.

15. The process as defined in Claim 14, wherein the conductive etch stop barrier layer is about 300 Å.

16. The process as defined in Claim 12, further comprising:

forming a diffusion barrier before forming the conductive etch stop barrier layer such that the diffusion barrier is formed between the conductive etch stop barrier layer and the substrate with the patterned magneto-resistive bit structure; and

wherein patterning the conductive etch stop barrier layer further comprises patterning the diffusion barrier.

17. The process as defined in Claim 16, wherein the diffusion barrier comprises Ta.

18. The process as defined in Claim 17, wherein the diffusion barrier is about 100 Å in thickness.

19. The process as defined in Claim 16, wherein the diffusion barrier comprises TaN.

20. The process as defined in Claim 12, further comprising:

forming a diffusion barrier comprising Ta before forming the conductive etch stop barrier layer such that the diffusion barrier is formed between the conductive etch stop barrier layer and the substrate with the patterned magneto-resistive bit structure, wherein the conductive etch stop barrier layer comprises CrSi, and wherein the substrate further comprises a monolithic integrated circuit; and

wherein patterning the conductive etch stop barrier layer further comprises patterning the diffusion barrier.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.

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Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Michael S. Okamoto
Registration No. 47,831
Attorney of Record
Customer No. 20,995
(310) 551-3450

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